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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,225	12/15/2003	Ha Ryong Yoon	40296-0047	8668
26633	7590	06/22/2006	EXAMINER	
HELLER EHRMAN WHITE & MCAULIFFE LLP 1717 RHODE ISLAND AVE, NW WASHINGTON, DC 20036-3001			PATEL, ANAND B	
			ART UNIT	PAPER NUMBER
			2116	

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/734,225	Applicant(s) YOON, HA RYONG	
	Examiner Anand Patel	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Preliminary Amendment filed 12/15/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 5-8, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No 6496445 to Lee.

- As per claim 1, Lee discloses a subsystem comprising:
 - A master (410) comprising a clock generator (column 6, lines 50-55) for generating a first clock signal (CLK1) and a second clock signal (CLK2) which have different frequencies from each other (column 5, line 63 – column 6, line 12; column 6, lines 55-61); and
 - A plurality of slaves (401-408) for receiving command and address signals from the master and transmitting data signals to the master (figure 4),
 - Wherein the first clock signal is used for the command and address signals (column 7, lines 1-7, 18-35), and the second clock signal is used for the data signals (column 7, lines 7-9, 18-35).
- As per claim 2, Lee discloses the subsystem wherein the master transmits command and address signals into the corresponding slave only at a rising edge of the first clock signal (column 7, lines 24-27).

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- As per claim 5, Lee discloses the subsystem wherein the slave is a memory module (401-408).
- As per claim 6, Lee discloses the subsystem wherein the frequency of the first clock signal is lower than that of the second clock signal (column 5, line 65 – column 6, line 1).
- As per claim 7, Lee discloses the subsystem wherein the clock generator is a clock synchronization means (920).
- As per claim 8, Lee discloses the subsystem wherein the clock generator further comprises a divider for dividing the first clock signal to generate the second clock signal (inherent given column 5, line 63 – column 6, line 12).
- As per claim 10, Lee discloses the subsystem wherein the clock synchronization means is a phase locked loop circuit (920).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of US Patent No 5345562 to Chen.

- As per claim 3, Lee fails to disclose the subsystem wherein the master transmits command and address signals into the corresponding slave only at a falling edge of the first clock signal. Chen teaches wherein the command and address signals are transmitted only at a falling edge of the clock signal (column 6, lines 17-22). An advantage of the system taught by Chen is the ability to ensure that equal access is given to write and read operations

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(column 4, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Lee with Chen. Motivation to modify is to increase system efficiency by ensuring proper scheduling.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of US Patent No 5963502 to Watanabe et al (Watanabe).

- As per claim 4, Lee fails to disclose the subsystem wherein the master transmits command and address signals into the corresponding slave at the rising and falling edges of the first clock signal. Watanabe teaches wherein the command and address signals are transmitted at the rising and falling edges of the clock signal (column 1, lines 58-63). An advantage of the system taught by Watanabe is the ability to ensure proper timing of the memory system with regards to operating conditions (column 9, line 66 – column 10, line 13). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Lee with Watanabe. Motivation to modify is to increase system reliability by ensuring proper timing.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of US Patent No 5671258 to Burns et al (Burns).

- As per claim 9, Lee discloses the subsystem wherein the clock generator (column 6, lines 50-55) produces a first clock signal (CLK1) and a second clock signal (CLK2). Lee fails to disclose drivers for driving the clock signals. Burns teaches multiple clock drivers, each driving a clock signal (column 2, lines 47-52). An advantage of the system taught by Burns is the ability to recover a clock signal without extra circuitry and wiring (column 2, lines 15-24). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Lee with Burns. Motivation to modify is to increase system reliability without increasing hardware costs.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on Mon-Fri 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ABP


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100